

**Doc. Number:**

- ☐ Tentative Specification  
☐ Preliminary Specification  
☒ Approval Specification

**MODEL NO.: N133BGE**  
**SUFFIX: P42**

**Customer:****APPROVED BY****SIGNATURE****Name / Title**

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
方健穎	曹文彬	歐陽志全
2012-02-16 15:43:35 CST	2012-02-10 14:46:10 CST	2012-02-10 11:09:37 CST

**CONTENTS**

<b>1. GENERAL DESCRIPTION .....</b>	<b>4</b>
1.1 OVERVIEW .....	4
1.2 GENERAL SPECIFICATIONS .....	4
<b>2. MECHANICAL SPECIFICATIONS .....</b>	<b>4</b>
2.1 CONNECTOR TYPE .....	4
<b>3. ABSOLUTE MAXIMUM RATINGS .....</b>	<b>5</b>
3.1 ABSOLUTE RATINGS OF ENVIRONMENT (BASEd on CMI Module) .....	5
3.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL) .....	5
3.3 ELECTRICAL ABSOLUTE RATINGS (OPEN CELL) .....	6
<b>4. ELECTRICAL SPECIFICATIONS .....</b>	<b>7</b>
4.1 TFT LCD OPEN CELL .....	7
4.2. INTERFACE CONNECTIONS .....	7
4.3 ELECTRICAL CHARACTERISTICS .....	9
4.4 LVDS INPUT SIGNAL TIMING SPECIFICATIONS .....	11
4.5 DISPLAY TIMING SPECIFICATIONS .....	13
4.6 POWER ON/OFF SEQUENCE .....	14
<b>5. OPTICAL CHARACTERISTICS .....</b>	<b>15</b>
5.1 TEST CONDITIONS .....	15
5.2 OPTICAL SPECIFICATIONS .....	15
<b>6. PACKING .....</b>	<b>18</b>
6.1 CMI OPEN CELL LABEL .....	18
6.2 PACKAGE RELIABILITY .....	19
6.3 CARTON .....	19
6.4 PALLET .....	20
<b>7. PRECAUTIONS .....</b>	<b>21</b>
7.1 HANDLING PRECAUTIONS .....	21
7.2 STORAGE PRECAUTIONS .....	21
7.3 OPERATION PRECAUTIONS .....	21
<b>Appendix. OUTLINE DRAWING</b>	

**REVISION HISTORY**

Version	Date	Page	Description
3.0	9.Feb, 2012	All	Approval spec Ver.3.0 was first issued.

## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

N133BGE-P42 is a 13.3 TFT Liquid Crystal Display with 30-pins-and-1ch-LVDS circuit board. This product supports 1366 x 768 HD mode and can display 262,144 colors. The backlight unit and converter are not built in.

### 1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	13.3 diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch	0.2148 (H) x 0.2148 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-

## 2. MECHANICAL SPECIFICATIONS

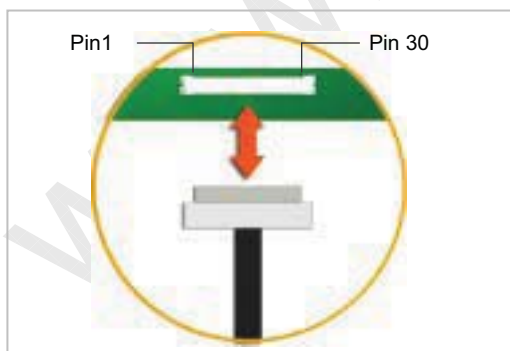
item		Min.	Typ.	Max.	Unit	Note
Size	Horizontal (H) with PCB	301.77	301.97	302.17	mm	(1) (2)
	Horizontal (H) w/o PCB	301.77	301.97	302.17	mm	
	Vertical (V) with PCB	190.74	191.24	191.74	mm	
	Vertical (V) w/o PCB	174.62	174.82	175.02	mm	
	Thickness (T) with PCB	-	1.9	2	mm	
	Thickness (T) w/o PCB	-	1.27		mm	
Weight (with polarizer release paper)		-	130	135	g	(1) (2)
I/F connector mounting position		The mounting inclination of the connector makes the screen center within $\pm 0.5\text{mm}$ as the horizontal.				

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

(2) Connector mounting position

### 2.1 CONNECTOR TYPE

#### 2.1.1 LVDS Connector



Please refer Appendix Outline Drawing for detail design.  
Connector Part No.: IPEX-20455-030E-12 or equivalent  
User's connector Part No: IPEX-20453-030T-01 or equivalent

#### 2.1.2 LED Light-Bar Connector

STM-MSK24036P8A



### 3. ABSOLUTE MAXIMUM RATINGS

#### 3.1 ABSOLUTE RATINGS OF ENVIRONMENT (Based on CMI Module)

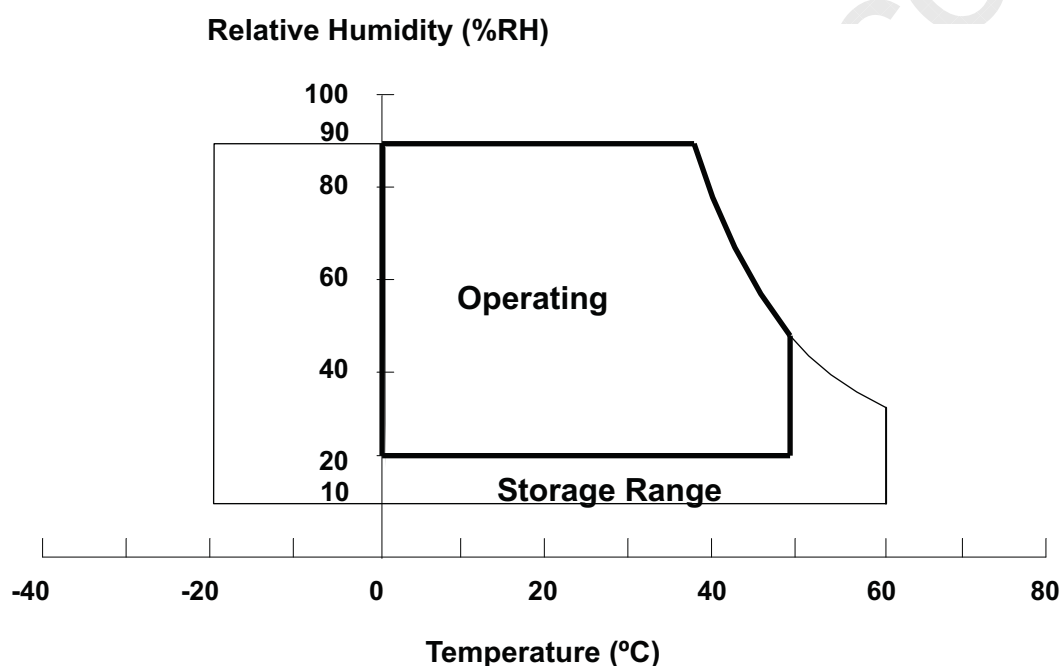
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T <sub>ST</sub>	-20	+60	°C	(1)
Operating Ambient Temperature	T <sub>OP</sub>	0	+50	°C	(1), (2)

Note (1) (a) 90 %RH Max. (Ta ≤ 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 °C min. and 60 °C max.



#### 3.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

High temperature or humidity may reduce the performance of panel. Please store LCD panel within the specified storage conditions.

Storage Condition: With packing.

Storage temperature range: 25±5 °C.

Storage humidity range: 50±10%RH.

Shelf life: 30days

**3.3 ELECTRICAL ABSOLUTE RATINGS (OPEN CELL)****3.3.1 TFT LCD MODULE**

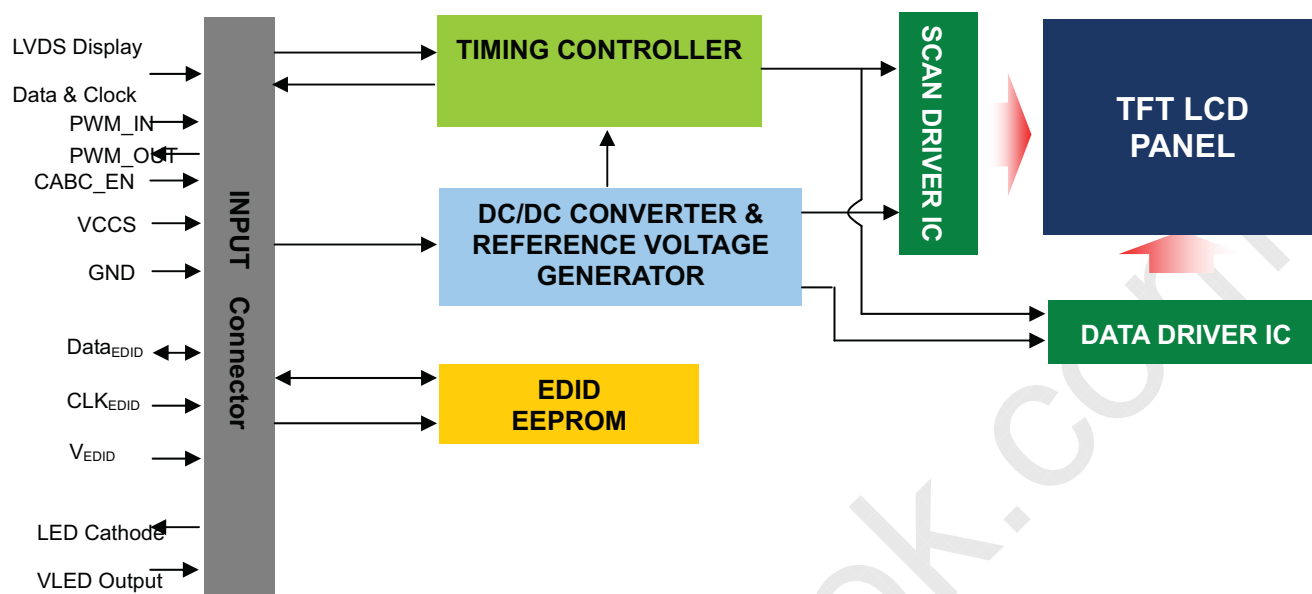
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V <sub>IN</sub>	-0.3	VCCS+0.3	V	
System PWM signal input for dimming	PWM_IN	-0.3	5	V	
Dynamic backlight control	CABC_EN	-0.3	5	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

www.panelook.com

## 4. ELECTRICAL SPECIFICATIONS

### 4.1 TFT LCD OPEN CELL



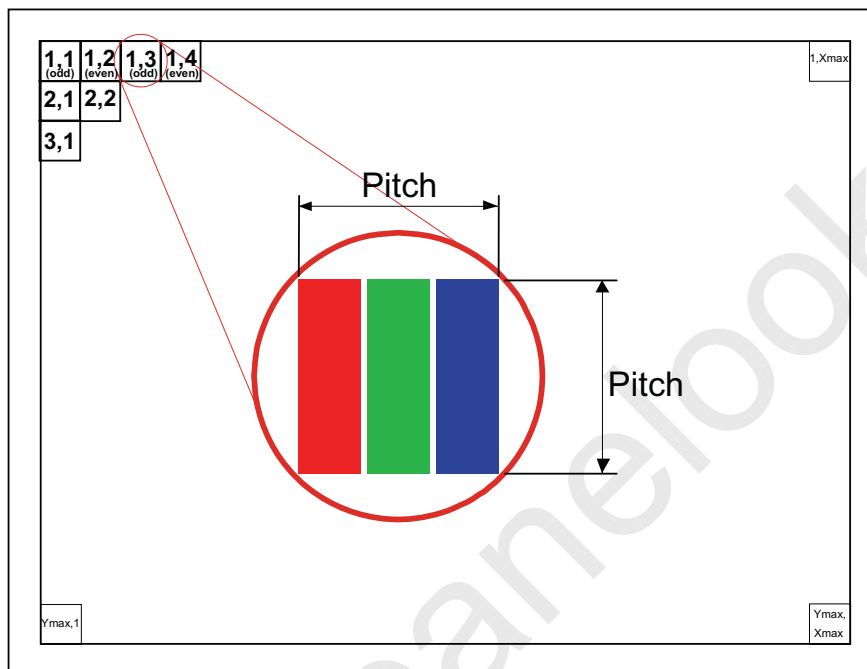
## 4.2. INTERFACE CONNECTIONS

### 4.2.1 PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserve)	
2	VCCS	Power Supply (3.3V typ.)	
3	VCCS	Power Supply (3.3V typ.)	
4	VEDID	DDC 3.3V power	
5	BIST	Panel self test	Bist
6	CLKEDID	DDC clock	
7	DATAEDID	DDC data	
8	Rxin0-	LVDS differential data input	R0-R5, G0
9	Rxin0+	LVDS differential data input	
10	VSS	Ground	
11	Rxin1-	LVDS differential data input	G1~G5, B0, B1
12	Rxin1+	LVDS differential data input	
13	VSS	Ground	
14	Rxin2-	LVDS Differential Data Input	B2-B5,HS,VS, DE
15	Rxin2+	LVDS Differential Data Input	
16	VSS	Ground	
17	RxCLK-	LVDS differential clock input	LVDS CLK
18	RxCLK+	LVDS differential clock input	
19	VSS	Ground	
20	PWM_IN	System PWM signal input for dimming	
21	CABC_EN	CABC Enable Input	
22	PWM_OUT	Panel PWM signal output to system	
23	NC	No Connection (Reserve)	

24	VLED Output	LED driver output	
25	VLED Output	LED driver output	
26	NC	No Connection (Reserve)	
27	LED_CA1	LED Cathode 1	
28	LED_CA2	LED Cathode 2	
29	LED_CA3	LED Cathode 3	
30	LED_CA4	LED Cathode 4	

Note (1) The first pixel is odd as shown in the following figure.



Note (2) The setting of CABC function are as follows.

Pin	Enable	Disable
CABC_EN	Hi	Lo or Open

Hi = High level, Lo = Low level.

Note (3) The I<sup>2</sup>C structure of CLKEDID and DATAEDID uses multiple slave device and the device addresses are defined as follows. The EDID part is M24C02-RMC6TG and D-VCOM part is iML7978CL.

Component	Device Address							
	B7	B6	B5	B4	B3	B2	B1	WR
EEPROM	1	0	1	0	0	0	0	X
D-VCOM	1	0	0	1	1	1	1	X



## 4.2.2 LED CONVERTER OUTPUT PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	VLED Output	LED driver output	
2	VLED Output	LED driver output	
3	NC	No Connection (Reserve)	
4	LED_CA1	LED Cathode 1	
5	LED_CA2	LED Cathode 2	
6	LED_CA3	LED Cathode 3	
7	LED_CA4	LED Cathode 4	
8	NC	No Connection (Reserve)	

## 4.3 ELECTRICAL CHARACTERISTICS

### 4.3.1 TFT LCD OPEN CELL

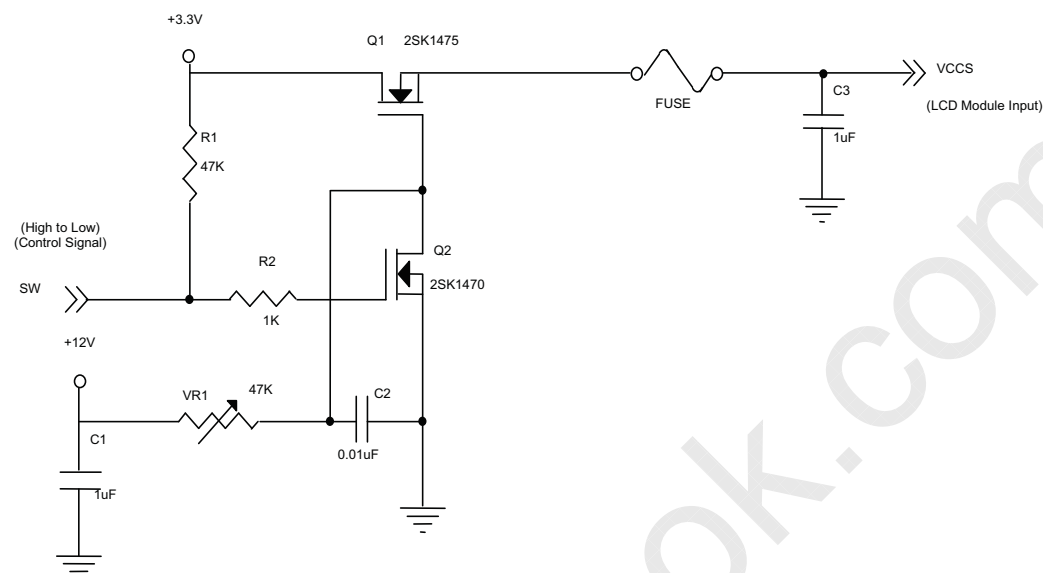
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)-
Ripple Voltage		V <sub>RP</sub>	-	50	-	mV	(1)-
CABC_EN Input Voltage	High Level	V <sub>IHCABC</sub>	2.3	-	3.6	V	
	Low Level	V <sub>ILCABC</sub>	0	-	0.5	V	
PWM Input Voltage	High Level	V <sub>IHCABC</sub>	2.3	-	3.6	V	
	Low Level	V <sub>ILCABC</sub>	0	-	0.5	V	
PWM Input Frequency		f <sub>PWM</sub>	190	-	2K	Hz	
PWMO Output Voltage	High Level	V <sub>IHCABC</sub>	2.0	-	2.8	V	
	Low Level	V <sub>ILCABC</sub>	0	-	0.4	V	
PWM Output Frequency		f <sub>PWM</sub>	190	-	2K	Hz	
Inrush Current		I <sub>RUSH</sub>	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	I <sub>CC</sub>	-	170	190	mA	(3)a
	Black		-	200	230	mA	(3)b

Note (1) The ambient temperature is Ta = 25 ± 2 °C.

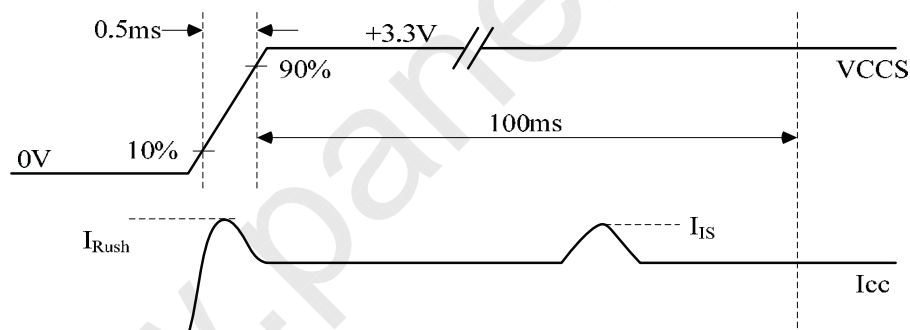
Note (2)  $I_{RUSH}$ : the maximum current when VCCS is rising

$I_{IS}$ : the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

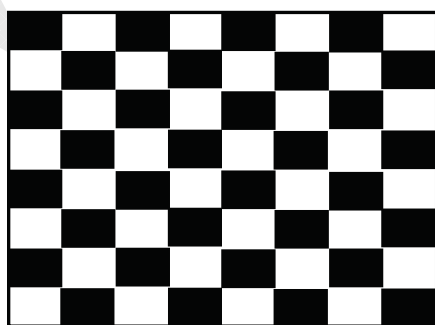


**VCCS rising time is 0.5ms**



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V,  $T_a = 25 \pm 2^\circ\text{C}$ , DC Current and  $f_v = 60\text{ Hz}$ , whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. Black Pattern



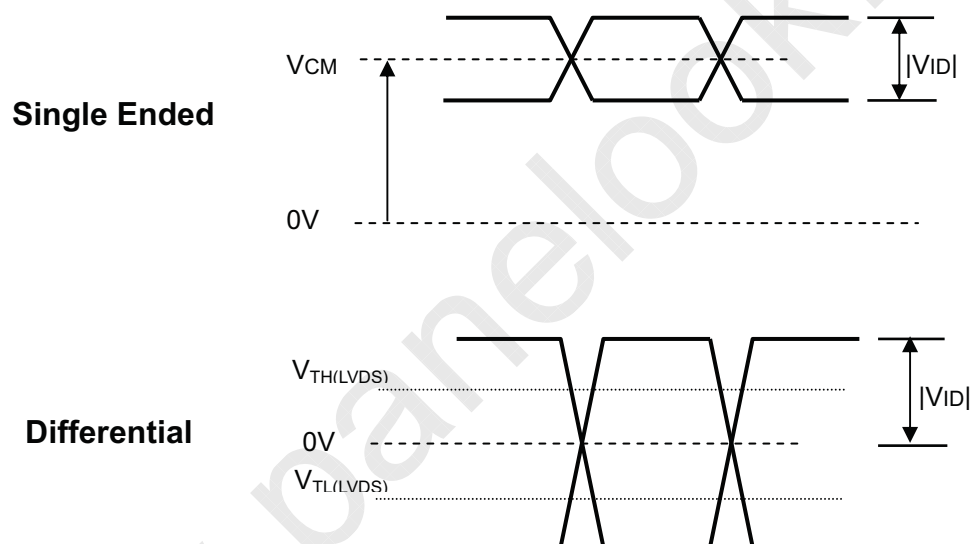
Active Area

## 4.4 LVDS INPUT SIGNAL TIMING SPECIFICATIONS

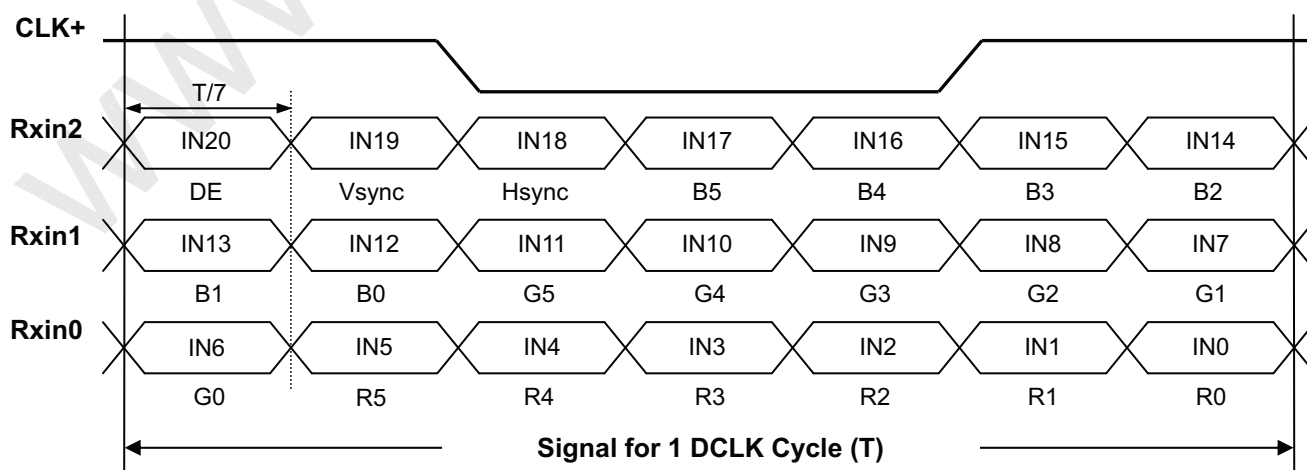
### 4.4.1 LVDS DC SPECIFICATIONS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LVDS Differential Input High Threshold	$V_{TH(LVDS)}$	-	-	+100	mV	(1), $V_{CM}=1.2V$
LVDS Differential Input Low Threshold	$V_{TL(LVDS)}$	-100	-	-	mV	(1), $V_{CM}=1.2V$
LVDS Common Mode Voltage	$V_{CM}$	1.125	-	1.375	V	(1)
LVDS Differential Input Voltage	$ V_{ID} $	100	-	600	mV	(1)
LVDS Terminating Resistor	$R_T$	-	100	-	Ohm	-

Note (1) The parameters of LVDS signals are defined as the following figures.



### 4.4.2 LVDS DATA FORMAT



## 4.4.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

#### 4.5 DISPLAY TIMING SPECIFICATIONS

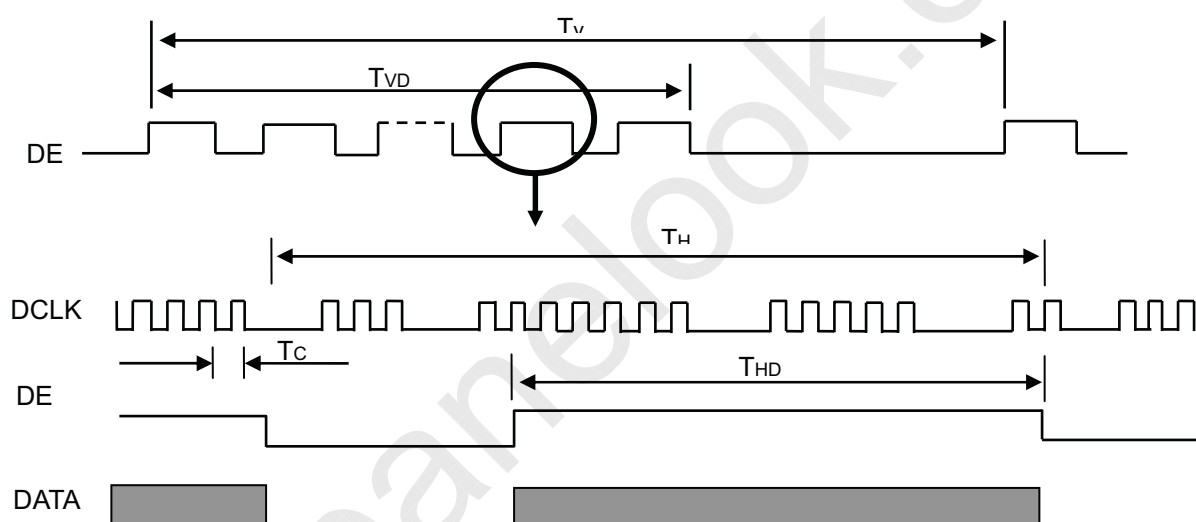
The input signal timing specifications are shown as the following table and timing diagram.

Refresh rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	50	75.44	80	MHz	-
DE	Vertical Total Time	TV	773	806	1008	TH	-
	Vertical Active Display Period	TVD	768	768	768	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	38	TV-TVD	TH	-
	Horizontal Total Time	TH	1448	1560	1950	Tc	-
	Horizontal Active Display Period	THD	1366	1366	1366	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	194	TH-THD	Tc	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

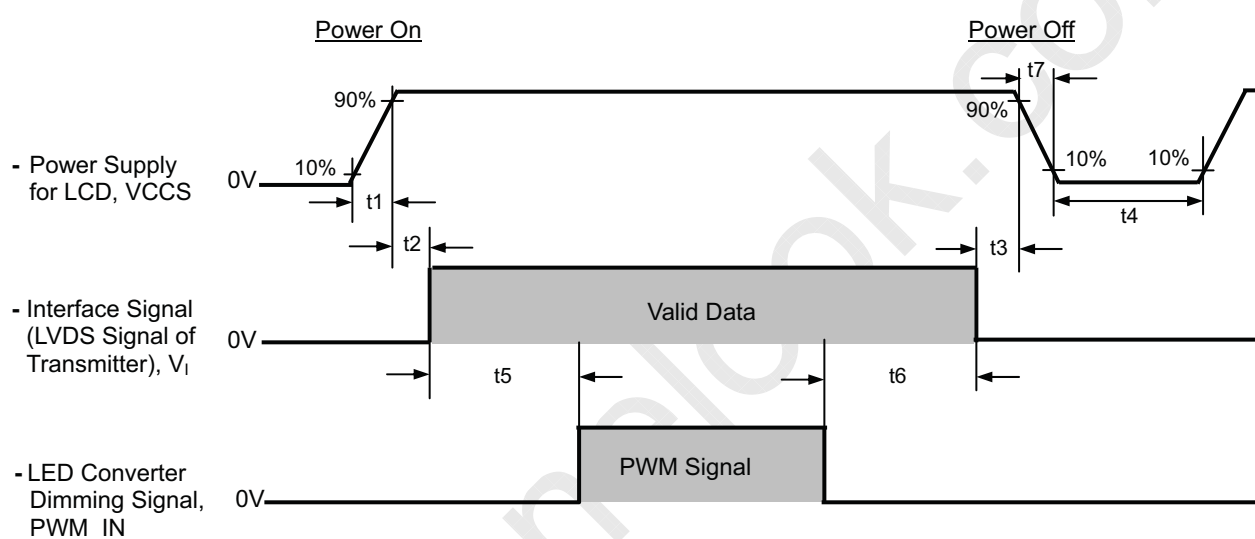
##### INPUT SIGNAL TIMING DIAGRAM



## 4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

Symbol	Value			Unit	Note
	Min.	Typ.	Max.		
t1	0.5	-	10	ms	
t2	0	-	50	ms	
t3	0	-	50	ms	
t4	500	-	-	ms	
t5	200	-	-	ms	
t6	200	-	-	ms	
t7	0.5	-	10	ms	



Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) Please avoid floating state of the interface signal during signal invalid period.

www.panelook.com

## 5. OPTICAL CHARACTERISTICS

### 5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V <sub>CC</sub>	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

### 5.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 5.1 and stable environment shown in Note (6).

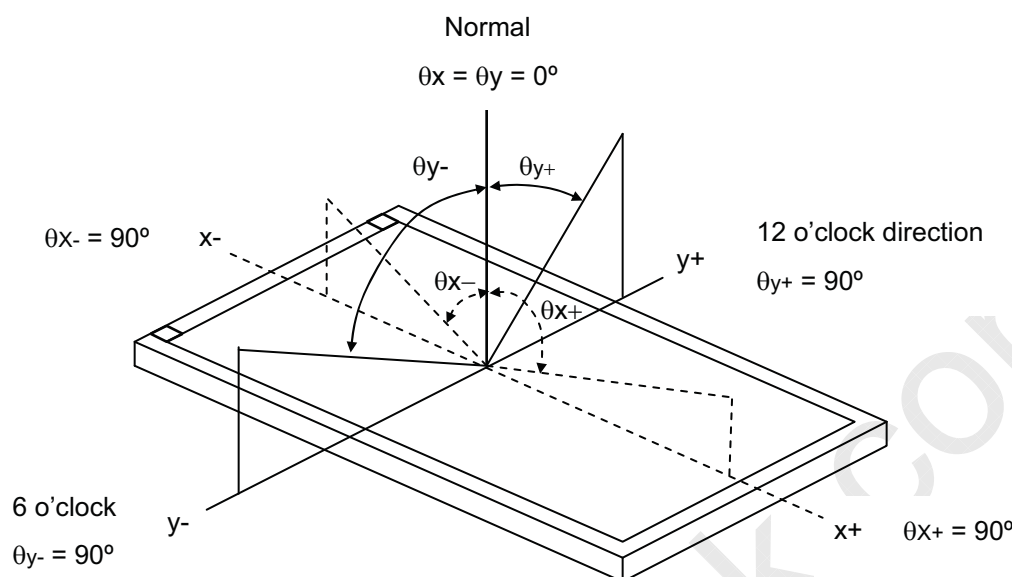
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	$\theta_x=0^\circ, \theta_Y=0^\circ$ CS-2000T Standard light source “C”	Typ - 0.03	0.601	Typ + 0.03	-	(0),(2), (5),(8)
		Rcy			0.326		-	
	Green	Gcx			0.289		-	
		Gcy			0.541		-	
	Blue	Bcx			0.145		-	
		Bcy			0.175		-	
	White	Wcx			0.295		-	
		Wcy			0.335		-	
Center Transmittance		T%	$\theta_x=0^\circ, \theta_Y=0^\circ$ CS-2000T, CMO BLU	5.9	6.5			(1),(2), (5),(7)
Contrast Ratio		CR		300	500		-	(2), (3)
Response Time		T <sub>R</sub>	$\theta_x=0^\circ, \theta_Y=0^\circ$		8	12	ms	(4)
		T <sub>F</sub>			8	13	ms	
Transmittance uniformity		δT%	$\theta_x=0^\circ, \theta_Y=0^\circ$ BM-5A			1.25	-	(2),(6)
Viewing Angle	Horizontal	θ <sub>x</sub> +	CR≥10 BM-5A	40	45			(2), (5)
		θ <sub>x</sub> -		40	45			
	Vertical	θ <sub>y</sub> +		15	20			
		θ <sub>y</sub> -		40	45			

Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltages are based on suitable gamma voltages. The calculating method is as following :

1. Measure Module's and BLU's spectrums. White is without signal input and R, G, B are with signal input. BLU is supplied by CMI.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C"

Note (1) Light source is the BLU which is supplied by CMI and driving voltages are based on suitable gamma voltages. White is without signal input and R, G, B are with signal input. Spec is judged by CMI's golden sample.

Note (2) Definition of Viewing Angle ( $\theta_x$ ,  $\theta_y$ ):



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

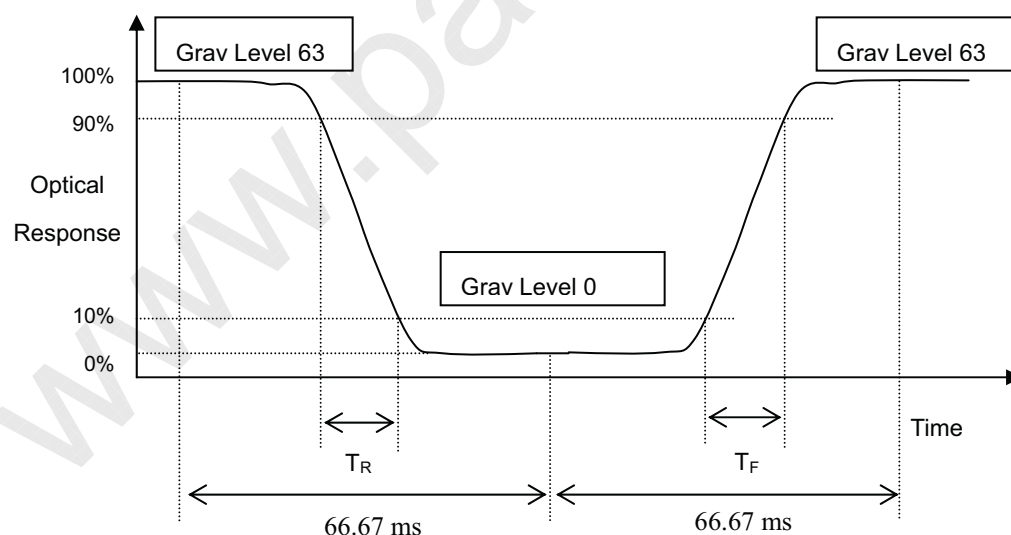
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

$$CR = CR(1)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

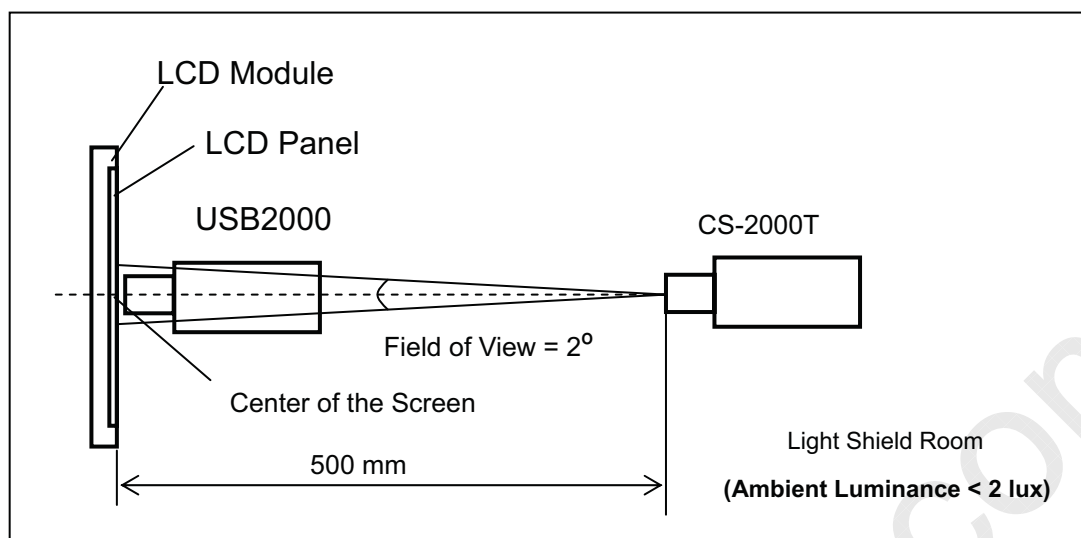
Note (4) Definition of Response Time ( $T_R$ ,  $T_F$ ):



Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.





Note (6) Definition of Transmittance Variation ( $\delta T\%$ ):

Measure the transmittance at 5 points

Maximum [ $T\%(1)$ ,  $T\%(2)$ , ...  $T\%(5)$ ]

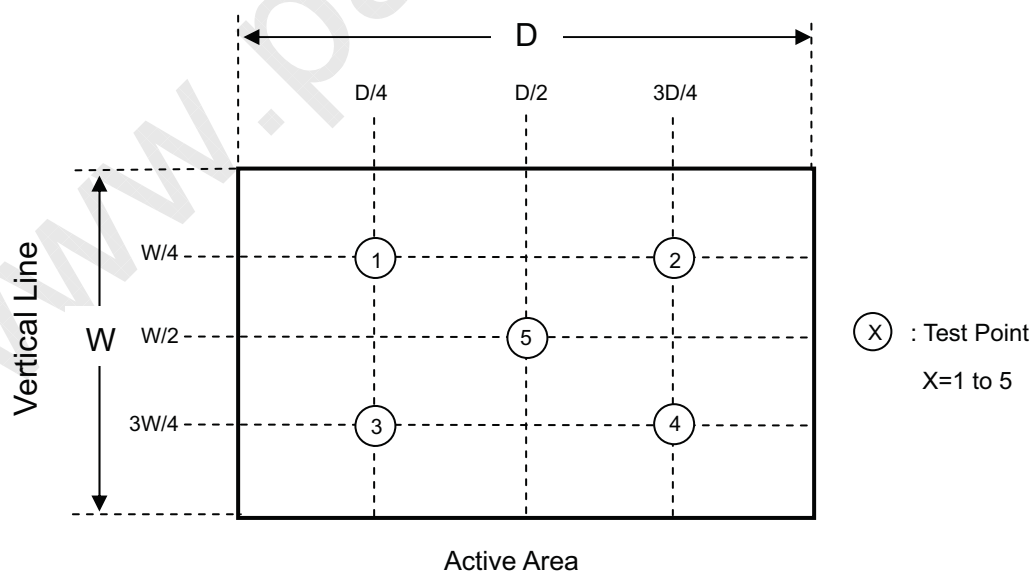
$$\delta T\% = \frac{\text{Maximum } [T\%(1), T\%(2), \dots T\%(5)]}{\text{Minimum } [T\%(1), T\%(2), \dots T\%(5)]}$$

Note (7) Definition of Transmittance ( $T\%$ ):

Module is without signal input.

BLU is supplied by CMI.

$$\text{Transmittance} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight Horizontal Line}} * 100\%$$



Note (8) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

## 6. PACKING

### 6.1 CMI OPEN CELL LABEL

The barcode nameplate is pasted on each OPEN CELL as illustration for CMI internal control.



(a) Model Name: N133BGE - P42

(b) Serial ID: XXXXXXYMDLNNNN

Serial No.

Product Line

Year, Month, Date

CMI Internal Use

Revision

CMI Internal Use

Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1<sup>st</sup> to 31<sup>st</sup>, exclude I, O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

## 6.2 PACKAGE RELIABILITY

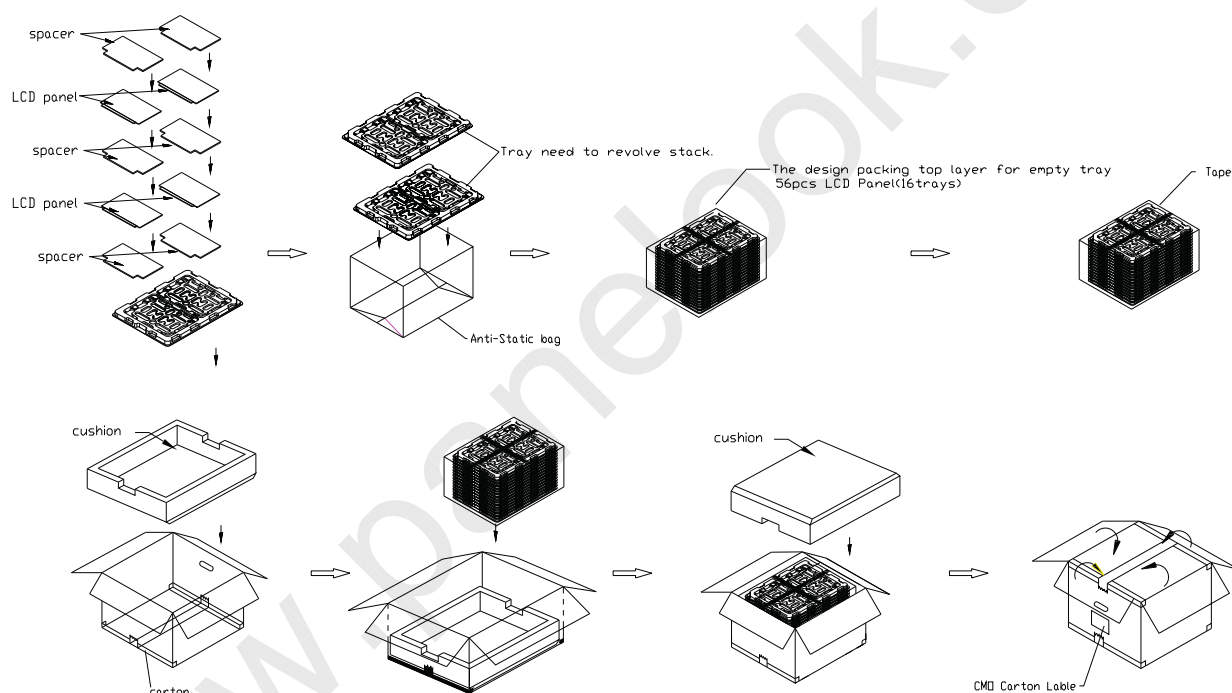
(1) Carton Packing should have no failure in the following reliability test items

Test Item	Test Conditions	Note
Packing Vibration	ISTA STANDARD Random, Frequency Range: 1 – 200 Hz Top & Bottom: 30 minutes (+Z), 10 min (-Z), Right & Left: 10 minutes (X) Back & Forth 10 minutes (Y)	Non Operation

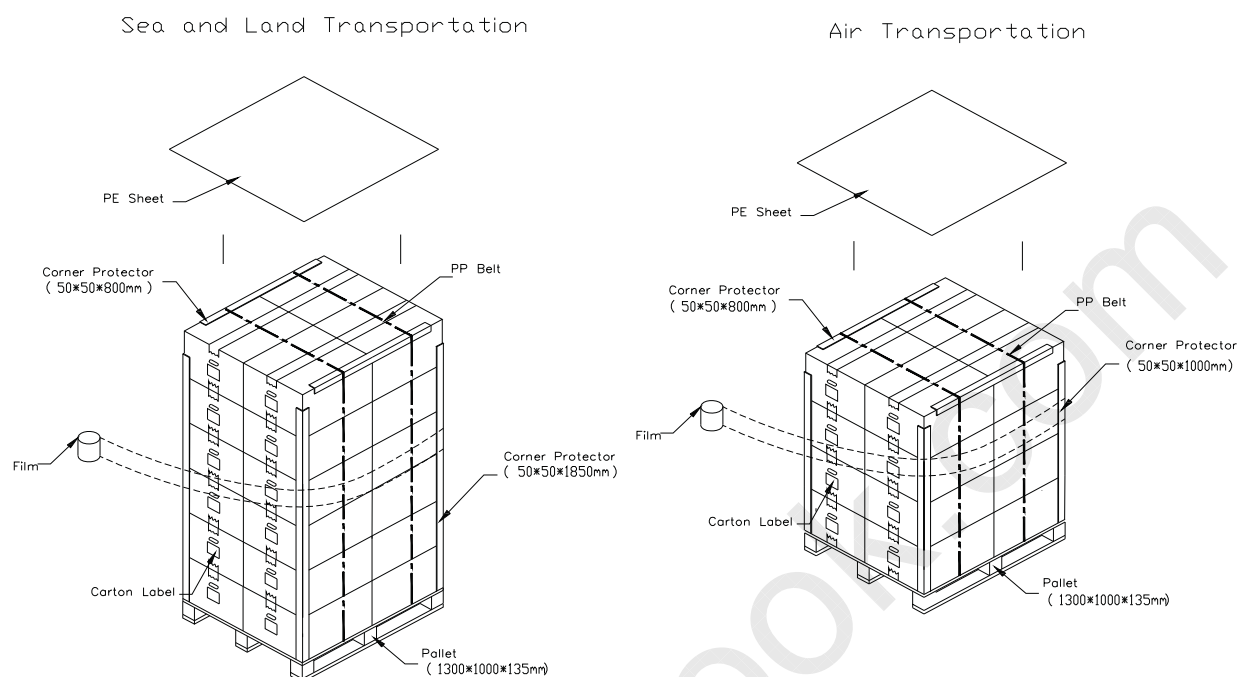
## 6.3 CARTON

(1) Carton Dimensions: 650(L)x495(W)x320(H)mm

(2) 56 LCD Cells+PCB/Carton



**Figure. 6-3 Packing method**

**6.4 PALLET****Figure. 6-4 Packing method**

## **7. PRECAUTIONS**

### **7.1 HANDLING PRECAUTIONS**

- (1) The open cell should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the open cell.
- (2) While assembling or installing open cell, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the open cell from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the open cell.
- (10) Pins of I/F connector should not be touched directly with bare hands.

### **7.2 STORAGE PRECAUTIONS**

- (1) High temperature or humidity may reduce the performance of open cell. Please store open cell within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the open cell, because the moisture may damage open cell when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly.

### **7.3 OPERATION PRECAUTIONS**

- (1) Do not pull the I/F connector in or out while the open cell is operating.
- (2) Always follow the correct power on/off sequence when open cell is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

**Appendix. OUTLINE DRAWING**